UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,351	12/02/2003	Herbert O. Ledebohm	19680-008100US	9024

20350 7590 06/22/2007

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
ZAMAN, FAISAL M	
ART UNIT	**PAPER NUMBER**
2111	

MAIL DATE	DELIVERY MODE
06/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/726,351	LEDEBOHM, HERBERT O.	
	Examiner	Art Unit	
	Faisal Zaman	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-19 and 21-23* is/are rejected.

7)☒ Claim(s) *7 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Claim Objections

1. Claim 23 recites the limitation "the registers" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-6, 13-15, 18, 19, 21, and 23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Diamant (U.S. Patent Publication No. 2004/0122997) in view of Benson et al. ("Benson") (U.S. Patent No. 5,542,076).

Regarding Claims 1, 14, and 21, Diamant discloses a method for servicing interrupts by a plurality of co-processors in a multiprocessor subsystem (Diamant, Figure 1, items 10a - 10n, Page 2, paragraph 20, the devices in Diamant are considered equivalent to the co-processors of the current application because both perform the function of processing data in the computing system), the method comprising the acts of:

In response to a detected interrupt, determining whether the detected interrupt was generated by one of the plurality of co-processors of the multiprocessor subsystem (Diamant, Page 4, paragraph 40); and

In the event that the detected interrupt was generated by one of the plurality of co-processors, scheduling execution of a deferred servicing procedure (Diamant, Page 4, paragraph 41);

Wherein during execution the deferred servicing procedure services a plurality of pending interrupts generated by one or more of the plurality of co-processors, including the detected interrupt (Diamant, Page 5, paragraph 43).

Diamant does not expressly teach wherein during execution, the deferred servicing procedure services a plurality of interrupts generated by two or more of the plurality of co-processors.

In the same field of endeavor (e.g. adaptively servicing interrupts received by a computer), Benson teaches wherein during execution, a deferred servicing procedure (Benson, Figure 2, item 70; ie. the interrupt servicing of interrupts received within the predetermined time period) services a plurality of interrupts generated by two or more of a plurality of co-processors (Benson, Figure 1, item 40, Column 6, lines 5-14; ie. devices 40 all send a plurality of interrupts to controller 30 within the predetermined time period, see Column 8, lines 30-33).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the Benson's teachings of adaptively servicing interrupts received by a computer with the teachings of Diamant, for the

purpose of not allowing controller activity to be substantially dominated by interrupt servicing when interrupts occur frequently (see Benson, Column 3, lines 12-15). Diamant provides motivation to combine by stating there is a need in the art to provide improved techniques for handling device interrupt requests (see Diamant, Page 1, paragraph 8).

Regarding Claim 2, Diamant discloses wherein during execution the deferred servicing procedure services all pending interrupts from all of the plurality of processors (Diamant, Figure 3, Page 6, Claim 5).

Regarding Claim 3, Diamant discloses wherein the plurality of pending interrupts serviced by the deferred servicing procedure includes a second interrupt generated by the one of the plurality of processors that generated the detected interrupt (Diamant, Figure 9, Page 5, paragraph 43, since there is a continuous loop that checks to see if another interrupt was generated from the device, it is understood that a second interrupt from the device could be serviced during the same deferred servicing procedure).

Regarding Claim 4, Diamant discloses wherein the plurality of pending interrupts serviced by the deferred servicing procedure includes a second interrupt generated by one of the plurality of processors other than the one that generated the detected interrupt (Diamant, Figure 3, Page 6, Claim 5, since there is a continuous loop

that checks to see if another interrupt was generated from the devices in the multiprocessor system, it is understood that a second interrupt from one of the devices could be serviced during the same deferred servicing procedure).

Regarding Claims 5 and 19, Diamant discloses wherein the act of determining whether the detected interrupt was generated by one of the plurality of co-processors includes the acts of:

Selecting one of the plurality of co-processors as a current co-processor (Diamant, Figure 8, Page 4, paragraph 40, the device which sends the interrupt begins the loop shown in Figure 8 and is therefore the current device); and

Reading a value stored in an interrupt register of the current co-processor (Diamant, Figure 1, items 14a – 14n, Page 2, paragraph 25).

Regarding Claim 6, Diamant discloses wherein the event that the value stored in the interrupt register does not indicate an interrupt, a different one of the co-processors is selected and the act of reading is repeated (Diamant, Figure 6, Page 4, paragraph 37).

Regarding Claims 13 and 18, Diamant discloses wherein the multiprocessor subsystem is a graphics processing subsystem (Diamant, Page 2, paragraph 0020; i.e., "video devices").

Regarding Claim 15, Benson teaches wherein the interrupt detection module is further configured to be activated by a central processing unit of the computer system in response to an interrupt signal (Benson, Figure 2, item 50, Column 5, lines 3-6).

The motivation that was used in the combination of Claim 1, super, applies equally as well to Claim 15.

Regarding Claim 23, Diamant teaches wherein servicing all pending interrupts from all of the plurality of co-processors comprises:

Loading by the deferred servicing procedure a mapping to the registers of a next co-processor to be serviced; and servicing any and all pending interrupts stored in the registers of the next co-processor (Diamant, Page 2, paragraph 0025; i.e., the device driver ISRs 20 comprise of a mapping of their associated status registers 14, and in response to receiving a call from the operating system ISR 16, check the status registers 14 and service any interrupts stored in them).

4. **Claims 10-12 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Diamant in view of Benson as applied to claim 1 above (hereinafter "Diamant-Benson"), and further in view of Simpson (U.S. Patent No. 5,867,687).

Diamant-Benson teaches the method of claim 1 as described above.

Regarding Claim 10, Diamant-Benson discloses the act of determining whether the detected interrupt was generated by one of the plurality of co-processors (Diamant, Page 4, paragraph 40).

Diamant-Benson does not expressly disclose wherein the act of determining whether the detected interrupt was generated by one of the plurality of co-processors is performed at a critical priority level.

In the same field of endeavor (e.g. control of multiple priority level interrupt requests to a CPU of a microprocessor), Simpson discloses a method for handling interrupts based on multiple priority levels (Simpson, Column 1 line 40 – Column 2 line 7).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the Simpson's teachings of control of multiple priority level interrupt requests to a CPU of a microprocessor with the teachings of Diamant-Benson, for the purpose of handling multiple priority level interrupt requests to a processor while reducing the problem of alteration to the processor itself (see Simpson, Column 1, lines 36-39). Also, it would have been desirable as stated by Simpson for interrupt processes to be able to be interrupted by higher priority interrupt processes (see Simpson, Column 2, lines 1-2).

Regarding Claim 11, Diamant-Benson discloses the act of scheduling execution of the deferred servicing procedure (Diamant, Page 4, paragraph 41).

Diamant-Benson does not expressly disclose wherein the act of scheduling execution of a deferred servicing procedure is performed at a critical priority level.

In the same field of endeavor, Simpson discloses a method for scheduling execution and deferring interrupts based on multiple priority levels (Simpson, Column 1, lines 40-61).

The motivation that was utilized in the combination of Claim 10, super, applies equally as well to Claim 11.

Regarding Claims 12 and 17, Diamant-Benson discloses the act of scheduling execution of a deferred servicing procedure (Diamant, Page 4, paragraph 41).

Diamant-Benson does not expressly disclose wherein the act of scheduling execution of a deferred servicing procedure includes setting a second priority level for the deferred servicing procedure, wherein the second priority level is lower than the critical priority level.

In the same field of endeavor, Simpson discloses a method for scheduling execution and deferring interrupts based on multiple priority levels (Simpson, Column 1, lines 40-61).

The motivation that was utilized in the combination of Claim 10, super, applies equally as well to Claim 12.

5. **Claims 8, 16, and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Diamant-Benson in view of Alasti et al. ("Alasti") (U.S. Patent No. 6,574,693).

Diamant-Benson teaches the method of claim 1 as described above.

Regarding Claims 8 and 16, Diamant-Benson teaches the act of disabling further interrupts from the co-processor in the event that the detected interrupt was generated by the co-processor (Diamant, Page 4, paragraph 0041), wherein during execution the deferred servicing procedure re-enables interrupts from the co-processor (Diamant, Figure 9, item 408, Pages 4-5, paragraph 42).

Diamant-Benson does not expressly teach the act of disabling further interrupts from the plurality of co-processors in the event that the detected interrupt was generated by one of the plurality of co-processors, wherein during execution the deferred servicing procedure re-enables interrupts from the plurality of co-processors.

In the same field of endeavor (e.g. processing interrupts within computers), Alasti teaches the act of disabling further interrupts from a plurality of co-processors in the event that a detected interrupt was generated by one of the plurality of co-processors, wherein during execution the deferred servicing procedure re-enables interrupts from the plurality of co-processors (Alasti, abstract, Column 5, lines 49-65; ie. interrupt gating modules 46 and 56 allow/deny interrupts to the processor based on the enable/disable signals).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Alasti's teachings of processing interrupts within computers with the teachings of Diamant-Benson, for the purpose of processing interrupts in a dynamic manner that allows for interrupt processing customization (see Alasti, Column 2, lines 31-35).

Regarding Claim 22, Diamant-Benson does not expressly teach determining whether interrupts from the plurality of co-processors are enabled; and if the interrupts from the plurality of co-processors are not enabled, exiting without performing further processing.

In the same field of endeavor, Alasti teaches determining whether interrupts from the plurality of co-processors are enabled; and if the interrupts from the plurality of co-processors are not enabled, exiting without performing further processing (Alasti, Column 5, lines 49-65; ie. interrupt gating modules 46 and 56 allow/deny interrupts to the processor based on the enable/disable signals).

The motivation that was used in the combination of Claim 8, super, applies equally as well to Claim 22.

6. **Claim 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over Diamant-Benson in view of Alasti as applied to claim 8 above (hereinafter "DBA"), and further in view of Simpson.

DBA teaches the method of claim 8 as described above.

Regarding Claim 9, DBA teaches the act of disabling further interrupts from a plurality of co-processors in the event that a detected interrupt was generated by one of the plurality of co-processors, wherein during execution the deferred servicing procedure re-enables interrupts from the plurality of co-processors (Alasti, abstract, Column 5, lines 49-65; ie. interrupt gating modules 46 and 56 allow/deny interrupts to the processor based on the enable/disable signals).

DBA does not expressly teach wherein the act of disabling further interrupts is performed at a critical priority level.

In the same field of endeavor (e.g. control of multiple priority level interrupt requests to a CPU of a microprocessor), Simpson discloses a method for handling interrupts based on multiple priority levels (Simpson, Column 1 line 40 – Column 2 line 7).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the Simpson's teachings of control of multiple priority level interrupt requests to a CPU of a microprocessor with the teachings of DBA, for the purpose of handling multiple priority level interrupt requests to a processor while reducing the problem of alteration to the processor itself (see Simpson, Column 1, lines 36-39). Also, it would have been desirable as stated by Simpson for interrupt processes to be able to be interrupted by higher priority interrupt processes (see Simpson, Column 2, lines 1-2).

Allowable Subject Matter

7. **Claims 7 and 20** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claim 7, the prior art of record does not teach updating a private register mapping to enable access to an interrupt register of a co-processor, wherein the private mapping is not used by a deferred servicing procedure.

Regarding Claim 20, the prior art of record does not teach wherein an interrupt detection module is configured to maintain a private mapping for accessing interrupt registers, the private mapping being used exclusively by the interrupt detection module.

Response to Arguments

9. Applicant's arguments filed 6/1/2007 have been fully considered but they are not persuasive. Regarding Claim 1, Applicant argues that "only one interrupt is serviced during execution of the interrupt process", and further "even when groups of interrupts are received, separate servicing procedures are performed for each interrupt" and "each interrupt is serviced by a separate interrupt process." The examiner respectfully disagrees. Contrary to Applicant's argument, Benson does in fact teach wherein "a deferred servicing procedure services a plurality of interrupts generated by two or more of a plurality of co-processors". First, with regards to the limitation "two or more processors", this is clearly taught in Figure 1, with items 40 all transmitting interrupts to controller 30. This is further described in Column 8, lines 30-33 ("counting interrupts *from a plurality of ancillary devices* occurring within the predetermined time period *while interrupt servicing is enabled*"). With regards to the claimed "deferred servicing procedure", as discussed in the previous Office Action, the servicing of interrupts that only arrive within the predetermined time period is considered equivalent to the

"deferred servicing procedure". Thus, it can clearly be seen that all interrupts that are received within the predetermined time period are in fact serviced by the controller 30. See for example, Figure 3, item 270 and Column 5 line 57 – Column 6 line 4 ("[a]s long as Nc, represented by the number in interrupt counter 160, is less than the threshold value THLD, *controller 30 continues to process the interrupts*"). Also see Figure 4, item 280 and Column 6, lines 12-14 ("controller 30 services an interrupt o*r a group of consecutive interrupts* and then returns to its other tasks").

Therefore, the claims stand as previously rejected.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal Zaman whose telephone number is 571-272-6495. The examiner can normally be reached on Monday thru Friday, 8 am - 5:30 pm, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

FMZ

Faisal Zaman
Examiner
Technology Center 2100

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100